IN THE CLAIMS

What is claimed is:

1. A method comprising:

forming a metal layer on a substrate, the metal layer having a thickness; and

exposing part of the metal layer to a wet etch chemistry that comprises an active ingredient with a diameter that exceeds the thickness of the metal layer.

2. The method of claim 1 wherein the thickness of the metal layer is less than about 100 angstroms.

3. The method of claim 1 wherein the metal layer comprises a material selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel, a metal carbide, and a conductive metal oxide.

4. The method of claim 1 wherein the wet etch chemistry comprises a hydrated etchant.

5. The method of claim 4 wherein the wet etch chemistry comprises an aqueous solution that includes between about 0.5 and about 5.0 moles/liter of a chelating agent.

6. A method for making a semiconductor device comprising:

forming a high-k gate dielectric layer on a substrate;

forming a metal layer on the high-k gate dielectric layer, the metal layer being less than about 100 angstroms thick;

forming a masking layer on the metal layer, exposing part of the metal layer; and

applying a wet etch chemistry that comprises an aqueous solution that includes between about 0.5 and about 5.0 moles/liter of a chelating agent to remove the exposed part of the metal layer from the high-k gate dielectric layer without removing more than about 100 angstroms of the metal layer from beneath the masking layer.

7. The method of claim 6 wherein the metal layer comprises a material selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel, a metal carbide, and a conductive metal oxide.

8. The method of claim 6 wherein the high-k gate dielectric layer comprises a material selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

9. The method of claim 6 wherein the masking layer comprises polysilicon.

10. The method of claim 6 wherein the metal layer is between about 25 angstroms and about 50 angstroms thick.

11. A method for making a semiconductor device comprising:

forming a high-k gate dielectric layer on a substrate;

forming a metal layer on the high-k gate dielectric layer, the metal layer being between about 25 angstroms and about 50 angstroms thick;

forming a polysilicon containing layer on the metal layer;

removing a first portion of the polysilicon layer to expose part of the metal layer; and

applying a wet etch chemistry that comprises an aqueous solution that includes between about 0.5 and about 5.0 moles/liter of a chelating agent to remove the exposed part of the metal layer from the high-k gate dielectric layer without removing more than about 100 angstroms of the metal layer from beneath the polysilicon containing layer.

12. The method of claim 11 wherein the high-k gate dielectric layer comprises a material selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.

13. The method of claim 11 wherein the metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV.

14. The method of claim 11 wherein the metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV.

15. The method of claim 11 wherein the chelating agent is a hexa-dentate chelating agent that is selected from the group consisting of carboxylic acid based chelating agents, phosphonic acid based chelating agents, and phenol derivatives.

16. A method for making a semiconductor device comprising:

forming a high-k gate dielectric layer on a substrate, the high-k gate dielectric layer comprising a material selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide;

forming a first metal layer on the high-k gate dielectric layer, the first metal layer being between about 25 angstroms and about 50 angstroms thick;

removing a first portion of the first metal layer;

forming a second metal layer on the high-k gate dielectric layer, the second metal layer being between about 25 angstroms and about 50 angstroms thick, a first portion of the second metal layer covering the remaining portion of the first metal layer and a second portion of the second metal layer covering the high-k gate dielectric layer;

forming a polysilicon containing layer on the second metal layer;

removing a first portion of the polysilicon layer selectively to the second metal layer to expose part of the second metal layer; and

removing the exposed part of the second metal layer and the underlying part of the first metal layer selectively to the high-k gate dielectric layer by exposing the second metal layer and the first metal layer to a wet chemistry that comprises an aqueous solution that includes between about 0.5 and about 5.0 moles/liter of a hexa-dentate chelating agent that is selected from the group consisting of carboxylic acid based chelating agents, phosphonic acid based chelating agents, and phenol derivatives.

17. The method of claim 16 wherein the first metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV, comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and serves as a gate electrode for an NMOS transistor, and the second metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV, comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and serves as a gate electrode for a PMOS transistor.

18. The method of claim 16 wherein the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV, comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and serves as a gate electrode for a PMOS transistor, and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV, comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal oxide, and serves as a gate electrode for an NMOS transistor.

19. The method of claim 16 wherein less than about 100 angstroms of the second metal layer and the underlying part of the first metal layer are removed from beneath the polysilicon containing layer, when the exposed part of the second metal layer and the underlying part of the first metal layer are removed selectively to the high-k gate dielectric layer.

20. The method of claim 19 wherein less than about 50 angstroms of the second metal layer and the underlying part of the first metal layer are removed from beneath the polysilicon containing layer.